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Docket No.: 200208731-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Timothy C. Fischer et al.

Application No.: 10/679,725

Confirmation No.: 2881

Filed: October 6, 2003

Art Unit: 2115

For: CENTRAL PROCESSING UNIT WITH MULTIPLE CLOCK ZONES AND OPERATING METHODS

Examiner: D. Butler

CORRECTED APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under 37 C.F.R. § 41.37(a), this brief is filed in response to Notification of Non-Compliant Appeal Brief mailed March 21, 2007, which was originally filed within two months of the Notice of Appeal filed in this case on November 17, 2006, and is in furtherance of said Notice of Appeal.

The fees required under 37 C.F.R. § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal

VII. Argument
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X. Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Limited Partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 20 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 0
2. Claims withdrawn from consideration but not canceled: 0
3. Claims pending: 1-20
4. Claims allowed: 0
5. Claims rejected: 1-3, 9-11, and 15-17

C. Claims On Appeal

The claims on appeal are claims 1-3, 9-11, and 15-17.

IV. STATUS OF AMENDMENTS

Applicant did not file an Amendment after Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in the independent claims involved in this appeal, referring to the specification by page and line number, and to the drawings by reference characters, as required by 37 C.F.R. § 41.37. Each element of the claims is identified by a corresponding reference to the specification and drawings, where applicable. However, citation to passages in the specification and drawings does not imply that limitations from the specification and drawings should be read into the corresponding claim element.

The invention as claimed in claim 1 relates to a central processing unit with multiple clock zones (see, e.g., paragraph 0011, at lns. 3–5, and Figure 1, at 100). The central processing unit includes at least one sensor that generates a power signal indicative of a power supply voltage within each clock zone (see, e.g., paragraph 0013, at lns. 1-6, and Figure 1, at 102), a clock generator for providing a variable frequency clock to each clock zone (see, e.g., paragraph 0012, at lns. 1-3, and Figure 1, at 103), and a controller for controlling the operating frequency of each clock generator in response to each power signal and in response to frequency adjustment communications from other clock zones (see, e.g., paragraph 0013, at lns. 4-7, paragraph 0014, at lns. 1-3, paragraph 0015, at lns. 4-9, and Figure 2, at 101).

In certain embodiments of the invention described above, such as that of dependent claim 2, the controller is able to communicate frequency adjustments to other clock zones (see, e.g., paragraph 0014, at lns. 1-2, and Figure 3, at 305).

In other embodiments of the invention described above, such as that of dependent claim 3, the frequency adjustment communications require at least one clock cycle (see, e.g., paragraph 0014, at lns. 4-10).

In still other embodiments of the invention described above, such as that of dependent claim 9, the sensor is a thermal detector (see, e.g., paragraph 0013, at lns. 1-2).

The invention as claimed in claim 10 also relates to a method of operating a central processing unit with multiple clock zones (see, e.g., paragraph 0020, at lns. 1-2, and Figure 5). The method includes generating at least one power signal indicative of a power supply voltage within each clock zone (see, e.g., paragraph 0020, at lns. 2-4, and Figure 5, at 501), adjusting the frequency of a local clock in one clock zone in response to the power signal from that clock zone (see, e.g., paragraph 0020, at lns. 4-6, and Figure 5, at 503), communicating the clock zone frequency adjustment to a second clock zone (see, e.g., paragraph 0020, at lns. 6-7, and Figure 5, at 505), and adjusting the frequency of a local clock in the second clock zone in response to the first clock zone frequency adjustment (see, e.g., paragraph 0020, at lns. 7-8, and Figure 5, at 507).

In other embodiments of the method described above, such as that of dependent claim 11, communicating the clock zone frequency adjustment to the second clock zone requires at least one clock cycle (see, e.g., paragraph 0014, at lns. 4-10).

The invention as claimed in claim 15 also relates to a central processing unit with multiple clock zones (see, e.g., paragraph 0011, at lns. 3–5, and Figure 1, at 100) that includes, in each clock zone, a means for generating a power signal indicative of a power supply voltage within each clock zone (see, e.g., paragraph 0013, at lns. 1-6, paragraph 0017, at lns. 2-4, and Figure 1, at 102) and a means for modifying a frequency of a variable frequency clock in response to the power signal and in response to frequency adjustment communications from other clock zones (see, e.g., paragraph 0013, at lns. 3-7, paragraph 0014, at lns. 1-10, paragraph 0015, at lns. 4-9, paragraph 0016, at lns. 1-12, and Figure 2, at 101).

In other embodiments of the invention described above, such as that of dependent claim 16, the means for modifying a frequency also communicates frequency adjustments to other clock zones (see, e.g., paragraph 0014, at lns. 1-10, paragraph 0016, at lns. 1-9, and Figure 2, at 204).

In other embodiments of the invention described above, such as that of dependent claim 17, the frequency adjustment communication requires at least one cycle (see, e.g., paragraph 0014, at lns. 4-10).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 10, and 15 are rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1, 8, and 15 of U.S. Patent 7,076,679.

B. Whether claims 1, 2, 9, 15 and 16 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,047,248 to Georgiou et al. ("Georgiou").

C. Whether claim 10 is properly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,047,248 to Georgiou et al. ("Georgiou").

VII. ARGUMENT

A. Obviousness Type Double Patenting

Claims 1, 10, and 15 are rejected on the grounds of non-statutory obviousness-type double patenting as being unpatentable over claims 1, 8, and 15 of U.S. Patent 7,076,679. In response to this rejection, Appellant has previously stated that it would file a terminal disclaimer to overcome this rejection should the double patenting rejection apply to the claims as allowed. Response dated June 1, 2006, page 7.

B. Rejection of Claims 1, 2, 9, 10, 15 and 16 under 35 U.S.C. § 103(a)

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the applied reference. *See In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. *In re Merck and Co., Inc.,* 800 F.2d 1091, 231 U.S.P.Q. 375, 379 (Fed. Cir. 1986). Finally, the applied reference(s) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580, 583 (C.C.P.A. 1974). Without conceding the second criterion, Appellant respectfully asserts that the rejection does not satisfy first or the third criteria, as discussed further below.

Georgiou does not teach or suggest all of the claim limitations in independent claim 1 because Georgiou does not teach or suggest at least one sensor that generates a power signal indicative of a power supply voltage within the clock zone, or multiple clock zones where each clock zone includes a clock generator and a controller for controlling the operating frequency of the clock generator. Nor does Georgiou describe a controller for controlling the operating frequency of the clock generator in response to frequency adjustment communications from other clock zones.

1. Georgiou does not sense power supply voltage within the clock zone.

With regard the at least one sensor of claim 1, Appellee has referenced temperature sensors T1 through Tk from Figure 1 and column 3, lines 31-40 and column 4, lines 18-44. Georgiou is quite clear that the only sensor is a temperature sensor that generates an electrical signal representative of the temperature of the associated functional unit. Column 4, lines 18-21. Nowhere does Georgiou describe a sensor measuring a power supply voltage within the functional unit. While Georgiou does characterize the operation of each functional unit for different voltage/frequency pairs to prevent synchronization and reliability issues (column 4, lines 21-26), and using a voltage regulator that can reduce power supply voltage (column 4, lines 34-36), Georgiou does not describe at least one sensor that generates a power signal indicative of a power supply voltage within the clock zone as required by claim 1. Instead, Georgiou monitors the temperature of a functional unit and if the temperature exceeds a threshold, Georgiou reduces the operating voltage and/or the operating frequency to reduce the thermal output of the functional unit and thereby reduce the temperature of the functional unit. Column 3, lines 19-22.

2. Georgiou does not describe each clock zone including a clock generator and a controller.

With regard to the limitation in claim 1 of multiple clock zones, each clock zone including a clock generator and a controller for controlling the operating frequency of the clock generator, Appellee has cited column 5, lines 1-8 of Georgiou which describes a decoder 130, a regulator 330 and a selector 430 which are associated with each independently controllable functional unit. Such an arrangement is shown in Figure 1.

The Appellee states on page 6 of the Final Office Action that "Georgiou describes that the controller (decoder 130) controls each clock generator (clock selector 430) of each zone (functional unit and associated circuitry) and temperature decoder 130 (controller) include circuitry associated with each one of the functional units. Appellant respectfully asserts that the Appellee is mischaracterizing Georgiou when Appellee recites the controller controlling *each clock generator*. Georgiou clearly only shows a single clock selector 430, not a clock generator in each zone as required by claim 1.

If the Appellee is trying to equate the arrangement of Figure 1 with the limitations of claim 1 by stating that each of the individual elements (i.e. decoder 130, regulator 330 and clock selector 430) has dedicated circuitry and that the dedicated circuitry would meet the limitations of claim 1, Applicant respectfully disagrees. First, Appellee provides no support in Georgiou for his assertion that the blocks in questions contain dedicated circuitry for each zone, but instead reads teachings into Georgiou that are not required or implied by the teachings of Georgiou. Instead of the arrangement proposed by the Appellee, Georgiou may have universal circuitry that calculates the appropriate parameter and sends it to the functional unit. In fact, Figure 4 shows that the only common circuitry in the clock selector 430 is a multiplexor associated with each functional unit that is controlled to output a selected clock frequency for a functional unit. Column 8, lines 65-67. The multiplexor 470 is not a clock generator in each zone as required by claim 1.

3. There is no motivation modify Georgiou to include a controller responsive to frequency adjustment communications from other clock zones.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. M.P.E.P. § 2143.01 (citing *In re Mills*, 916 F.2d 680, (Fed. Cir. 1990)).

With regard to a controller for controlling the operating frequency of the clock generator in response to frequency adjustment communications from other clock zones as required by claim 1, Appellee admits that Georgiou fails to "explicitly" teach this limitation. Instead Appellee cites to column 4, lines 36-39 which recites that clock selector 430 cooperative modulates the clock frequency to maintain system synchronization and uses this sentence to justify modifying Georgiou.

Appellee states:

> Therefore, Georgiou discloses cooperatively adjusting the clock frequency in response to the temperature (power) signal such that system synchronization of the whole chip is maintained. It would have been obvious to one having ordinary skill in the art at the time the invention was made to control an operating frequency of the clock generator in response to communications from other clock zones as suggested by Georgiou in order to maintain synchronization f the whole chip. (Final Office Action, page 4)

First, Appellee equates temperature with power. While temperature may be related to the power consumed by a circuit, claim 1 recites sensing power supply voltage, not consumed power as implied by the Appellee. Second, Appellee omits from the citation of column 4, lines 36-39, which is used to justify the motivation to modify Georgiou the immediately preceding sentence. This sentence makes clear that the cooperative aspect to the clock selector operation is that the clock selector operates cooperatively with the voltage regulator 330 not other functional units. Column 4, lines 34-36. This cooperative operation produces voltage/frequency pairs which have been previously characterized to ensure stability and synchronization. See, column 4, lines 21-26, and lines 46-51 and column 5, lines 5-11.

Using pre-characterized voltage/frequency pairs to promote synchronization and reliability as described by Georgiou is clearly different than controlling the operating frequency of the clock generator in response to frequency adjustment communications from other clock zones as required by claim 1. Nowhere does Georgiou describe frequency adjustment communications from any of its functional units. As the Appellee's justification for the motivation stated in the Final Office Action is not supported by Georgiou, there can be no motivation in Georgiou to make the modifications suggested by the Appellee.

Further, in the Appellee's statement the language of the recited motivation is circular in nature, stating that it is obvious to make the modification (control an operating frequency of the clock generator in response to communications from other clock zones) because it is obvious to achieve the result (maintain synchronization of and reliability of the whole chip). Such language is merely a statement that the reference can be modified, and does not state any desirability for making the modification.

Still further, Georgiou recites specific mechanisms for achieving the result identified by the Examiner (pre-characterized voltage/frequency pairs) that are incompatible with change suggested by the Examiner. The modification would result in changes to the frequencies without corresponding changes to the operating voltages as required by Georgiou's invention. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 249 (C.C.P.A. 1959).

Independent claim 15 requires multiple clock zones, each clock zone including means for generating a power signal that is indicative of a power supply voltage within the clock zone and means for modifying a frequency of a variable frequency clock. For the reasons described with respect to claim 1, Georgiou does not describe at least these limitations.

As described above Georgiou only senses the temperature of each functional unit. While Georgiou does adjust the power supply voltage and the operating frequency, this is done in response only to the temperature measured by the temperature sensors and not in response to any sensing of the power supply voltage within a clock zone.

Nor, for the reasons set forth above, does Georgiou describe multiple clock zones, each clock including means for modifying a frequency of a variable frequency clock as required by claim 15. As described, Georgiou only includes a sensor in each of the functional units. The voltage regulator and clock selector are shared by each of the functional units as shown in Figure 1. Nor does Georgiou describe dedicated circuitry on any of the shared elements as claimed by the Appellee.

Finally, as the Examiner admits (Final Office Action, page 4), Georgiou does not describe means for modifying a frequency of a variable frequency clock in response to frequency adjustment communications from other clock zones. Georgiou does describe pre-characterized, cooperative voltage/frequency pairs to ensure synchronization and reliability, as set forth with respect to claim 1, but does not ever describe frequency adjustment communications from other clock zones. For the reasons described with respect to claim 1, the Appellee's proposed modification to Georgiou is based on a mischaracterization of Georgiou, namely that temperature is not equivalent to power supply voltage, and the "cooperatively adjusting" refers not to cooperation among functional units but cooperation between the voltage regulator and clock selector in obtaining a pre-characterized voltage/frequency pair. Additionally, the Appellee's proposed modification is circular in nature and would require changing the principle of operation of Georgiou.

For the reasons set forth above, Appellant respectfully asserts that claims 1 and 15 are allowable over the rejection of record and respectfully requests that the Board overturn the rejection of claims 1 and 15 under 35 U.S.C. § 103(a).

C. Rejection of Claim 10 under 35 U.S.C. § 103(a)

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the applied reference. *See In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. *In re Merck and Co., Inc.*, 800 F.2d 1091, 231 U.S.P.Q. 375, 379 (Fed. Cir. 1986). Finally, the applied reference(s) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580, 583 (C.C.P.A. 1974). Without conceding the second criterion, Appellant respectfully asserts that the rejection does not satisfy first or the third criteria, as discussed further below.

Claim 10 requires, in part, generating at least one power signal that is indicative of a power supply voltage within each of the clock zones, adjusting a frequency of a first local clock in response to a respective power signal from the first clock zone, communicating the first clock zone frequency adjustment to a second clock zone, and adjusting the frequency of a second local clock in a second clock zone in response to a frequency clock adjustment in a second clock zone.

As described above with respect to claim 1 and 15, Georgiou only senses the temperature of each functional unit. While Georgiou does adjust the power supply voltage and the operating frequency, this is done in response only to the temperature measured by the temperature sensors and not in response to any sensing of the power supply voltage within a clock zone. The Appellee at various times attempts to equate temperature with power in order to meet the limitations of claims 1, 10 and 15. While temperature may bear a relation to power consumption (relative activity of the circuit elements), it does not bear a relation to power supply voltage as required by claim 10.

Neither does Georgiou describe adjusting a frequency of a second local clock in a second local clock zone in response to the first clock zone frequency adjustment. For the reasons described with respect to claim 1, the Appellee's proposed modification to Georgiou is based on a mischaracterization of Georgiou, namely that temperature is not equivalent to power supply voltage, and the "cooperatively adjusting" refers not to cooperation among functional units but cooperation between the voltage regulator and clock selector in obtaining a pre-characterized voltage/frequency pair. Additionally, the Appellee's proposed modification is circular in nature and would require changing the principle of operation of Georgiou.

Appellant, therefore respectfully asserts that claim 10 is allowable over the rejection of record and respectfully requests that the Board overturn the rejection of claim 10 under 35 U.S.C. § 103(a).

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

Dated: April 18, 2007

I hereby certify that this document is being transmitted to the US Patent and Trademark Office via electronic filing.

Date of Deposit: April 18, 2007

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/679,725:

1. A central processing unit (CPU) that includes multiple clock zones, said CPU comprising:

in each clock zone,

at least one sensor that generates a power signal indicative of a power supply voltage within said clock zone;

a clock generator for providing a variable frequency clock to said clock zone; and

a controller for controlling an operating frequency of said clock generator in response to said power signal and in response to frequency adjustment communications from other clock zones.

2. The CPU of claim 1 wherein said controller is operable to communicate adjustments of said operating frequency performed in response to said power signal to other clock zones.

3. The CPU of claim 2 wherein communication of said frequency adjustments requires at least one clock cycle.

4. The CPU of claim 3 wherein, when a controller in a first clock zone receives a frequency adjustment communication from a second clock zone, said controller in said first clock zone adjusts an operating frequency of a clock generator of said first clock zone to drive a phase misalignment between said first clock zone and said second clock zone to zero.

5. The CPU of claim 4 wherein said controller in said first clock zone drives a frequency misalignment between said first clock zone and said second clock zone to zero after driving said phase misalignment to zero.

6. The CPU of claim 3 wherein a controller in a first clock zone does not communicate an adjustment of an operating frequency in said first clock zone when, in an immediately previous clock cycle, said controller in said first clock zone has received a frequency adjustment communication from a second clock zone.

7. The CPU of claim 3 wherein a controller in a first clock zone does not perform a frequency adjustment in response to a frequency adjustment communication from a second clock zone when said controller in said first clock zone has performed a frequency adjustment in response to a power signal from said first clock zone in an immediately previous clock cycle.

8. The CPU of claim 1 wherein said at least one sensor is a voltage detector.

9. The CPU of claim 1 wherein said at least one sensor is a thermal detector.

10. A method of operating a central processing unit (CPU) that comprises multiple clock zones, said method comprising:

generating at least one power signal that is indicative of a power supply voltage within each of said clock zones;

adjusting a frequency of a first local clock in a first clock zone of said clock zones in response to a respective power signal from said first clock zone;

communicating said first clock zone frequency adjustment to a second clock zone; and

adjusting a frequency of a second local clock in said second clock zone in response to said first clock zone frequency adjustment.

11. The method of claim 10 wherein said communicating said first clock zone frequency adjustment requires at least one clock cycle.

12. The method of claim 11 wherein said second zone frequency adjustment comprises:

driving a phase misalignment between said first clock zone and said second clock zone to zero.

13. The method of claim 12 wherein said second zone frequency adjustment comprises:

driving a frequency misalignment between said first clock zone and said second clock zone to zero after driving the phase misalignment to zero.

14. The method of claim 11 further comprising:

receiving, at the first clock zone, a frequency adjustment communication from a third clock zone in a clock cycle immediately subsequent to said first clock zone frequency adjustment; and

omitting adjustment of a frequency of a first local clock of said first clock zone in response to said third clock zone frequency adjustment.

15. A central processing unit (CPU) that includes multiple clock zones, said CPU comprising:

in each clock zone,

means for generating a power signal that is indicative of a power supply voltage within said clock zone; and

means for modifying a frequency of a respective variable frequency clock in response to said power signal and in response to frequency adjustment communications from other clock zones.

16. The CPU of claim 15 wherein said means for modifying a frequency communicates frequency adjustments to other clock zones.

17. The CPU of claim 16 wherein communication of frequency adjustments requires at least one clock cycle.

18. The CPU of claim 17 wherein a means for modifying a frequency in a first clock zone is operable to drive a phase misalignment between said first clock zone and a second clock zone to zero in response to a frequency adjustment communication from said second clock zone.

19. The CPU of claim 18 wherein said means for modifying in said first clock zone is operable to drive a frequency misalignment between said first clock zone and said second clock zone to zero after driving said phase misalignment to zero.

20. The CPU of claim 17 wherein a means for modifying a frequency in a first clock zone does not adjust a variable frequency clock in said first clock zone in response to a frequency adjustment communication from a second clock zone, if the second clock zone frequency adjustment communication is received in a clock cycle that is immediately subsequent to a frequency adjustment performed in said first clock zone in response to a power signal from said first clock zone.

APPENDIX B

No evidence pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or entered by or relied upon by Appellee is being submitted.

APPENDIX C

No related proceedings are referenced in II. above, and therefore, copies of decisions in related proceedings are not provided.